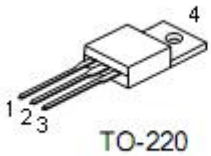
1. Applications

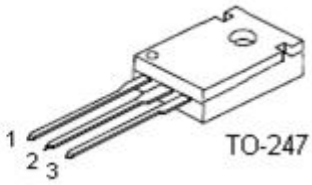
- DC-DC converters and Off-line UPS
- Switching applications

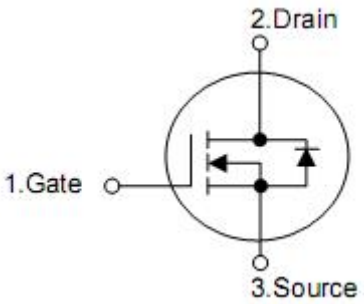
2. Features

- $R_{DS(on)\ (TYP)}$= 2.2mΩ @V_{GS}= 10 V
- Super high dense cell design
- Ultra low on-resistance
- 100% avalanche test
- Lead free and green devices available (RoHS compliant)

3. Pin configuration







Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Absolute maximum ratings

(T_C=25 ºC , unless otherwise specified)

Parameter		Symbol	Ratings		Units
Drain-source voltage		V_{DSS}	40		V
Gate-source voltage		V_{GSS}	±20		V
Operating and Storage temperature range		T_J &T_{STG}	-55~+175		˚C
Diode continuous forward current[1]	T_C=25 ºC	I_S	190		A
Continuous drain currenet V_{GS}= 10 V[1]	T_C=25 ºC	I_D	190		A
Continuous drain currenet V_{GS}= 10 V[1]	T_C=100 ºC		146		A
300us pulse drain current tested[2]	T_C=25 ºC	I_{DP}	760		A
Single pulse Avalanche energy		E_{AS}	812		mJ
Power dissipation	T_C=25 ºC	P_D	224	325	W
	T_C=100 ºC		112	162.5	W

5. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance,Junction-to-case	θ_{JC}	0.5	ºC/W

6. Electrical characteristics

(T_C=25°C,unless otherwise notes)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off Characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	40	-	-	V
Drain-to-source leakage current	I_{DSS}	V_{DS}=40V ,V_{GS}=0V	-	-	1	μA
		V_{DS}=40V , V_{GS}=0V,T_J=85 ºC	-	-	30	μA
Gate-to-source leakage current	I_{GSS}	V_{GS}=20V,V_{DS}=0V	-	-	100	nA
		V_{GS}=-20V,V_{DS}=0V	-	-	-100	nA
On characteristics						
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.0	3.0	4.0	V
Static drain-source on-resistance[4]	$R_{DS(on)}$	V_{GS}=10V,I_D=75A	-	2.2	3.5	mΩ
Dynamic characteristics						
Diode forward voltage	V_{SD}	V_{GS}=0V,I_S=75A	-	-	1.2	V
Reverse recovery time	t_{rr}	I_{SD}=75A,di_F/dt=100A/μs,	-	40	-	ns
Reverse recovery charge	Q_{rr}		-	52	-	nC
Gate resistance	R_G	V_{DS}=0V,V_{GS}=0V,f=1.0MHz	-	1.2	-	Ω
Input capacitance	C_{iss}	V_{DS}=20V,V_{GS}=0V,f=1.0MHz	-	4800	-	pF
Output capacitance	C_{oss}		-	950	-	pF
Reverse transfer capacitance	C_{rss}		-	480	-	pF
Total gate charge	Q_g	V_{Ds}=32V,I_D=75A,V_{GS}=10V,	-	120	-	nC
Gate-source charge	Q_{gs}		-	34	-	nC
Gate-drain (Miller)charge	Q_{gd}		-	46	-	nC
Resistve swiching characteristics		Essentially independent of operating temperature				
Turn-on-delay time	$t_{d(ON)}$	V_{DD}=20V,R_L=0.3Ω,I_D=75A, V_{GEN}=10V,R_G=2.5Ω	-	19	-	nS
Rise time	t_{rise}		-	96	-	
Turn-off-delay time	$t_{d(OFF)}$		-	70	-	
Fall time	t_{fall}		-	50	-	

Note: 1. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

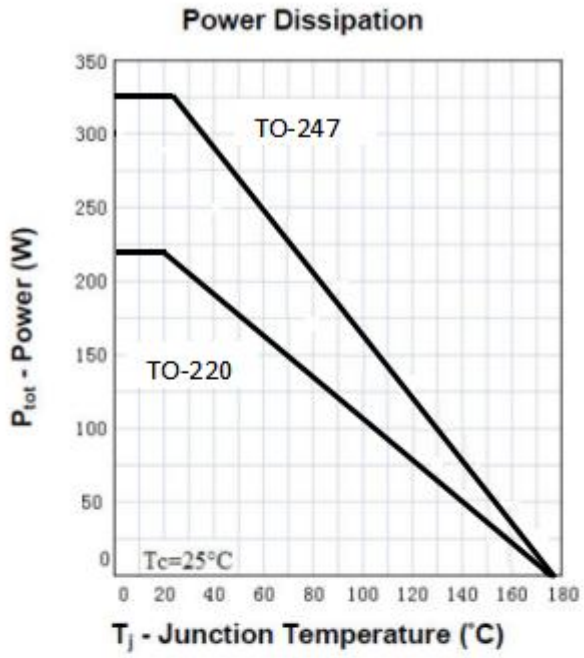
2. Pulse width limited by safe operating area.

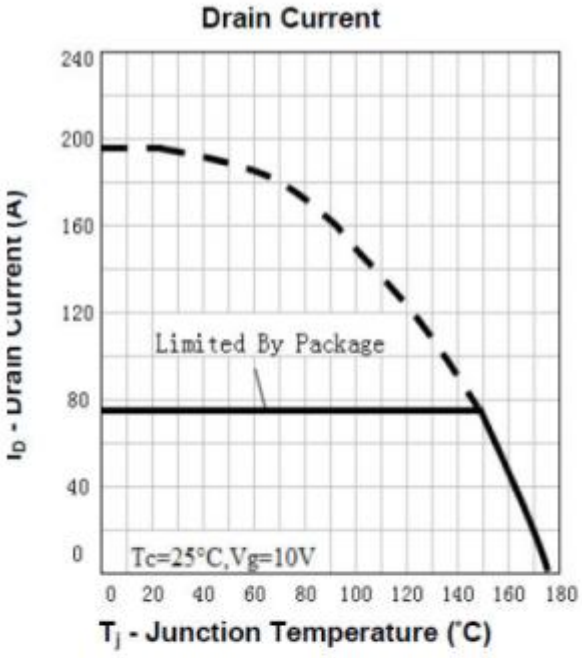
3. Limited by T_{Jmax}, I_{AS}=57A, V_{DD}=32V, R_G=50Ω, starting T_J=25 ºC.

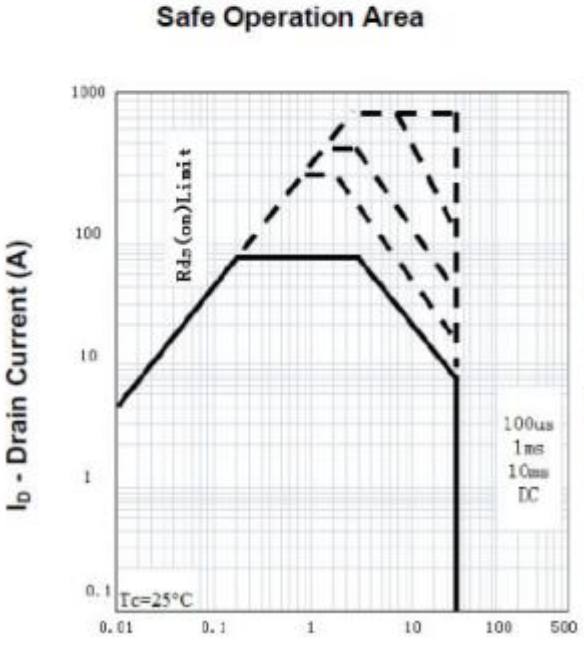
4. Pulse test; Pulse width ≤300μs; duty cycle ≤2%.

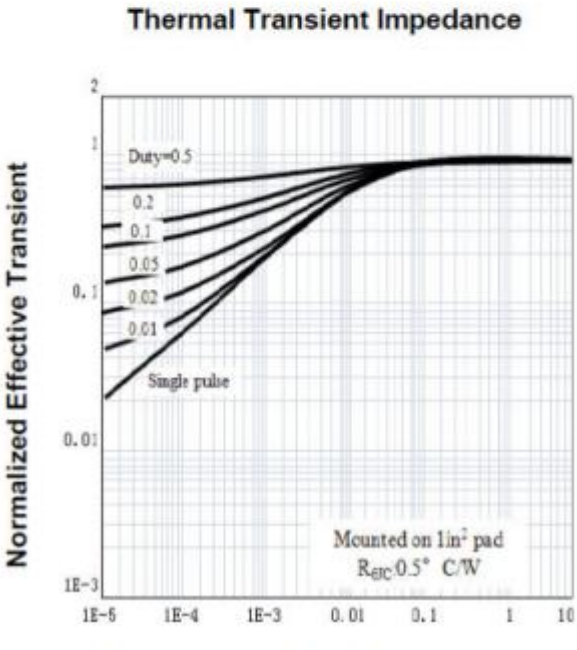
5. Guaranteed by design, not subject to production testing.

7. Test circuits and waveforms

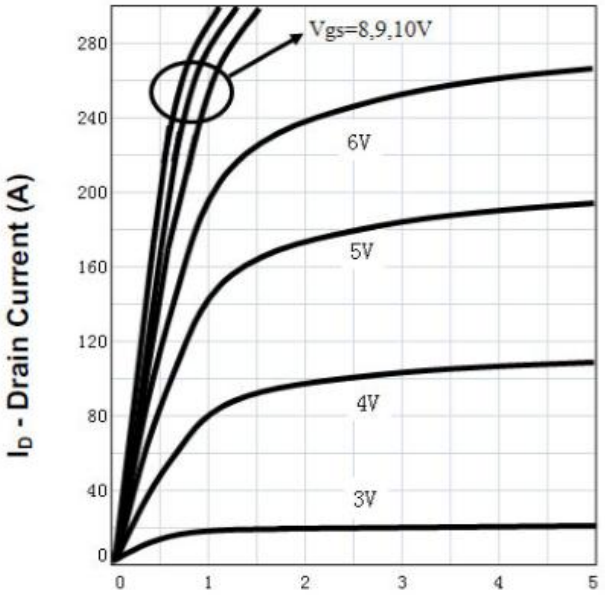




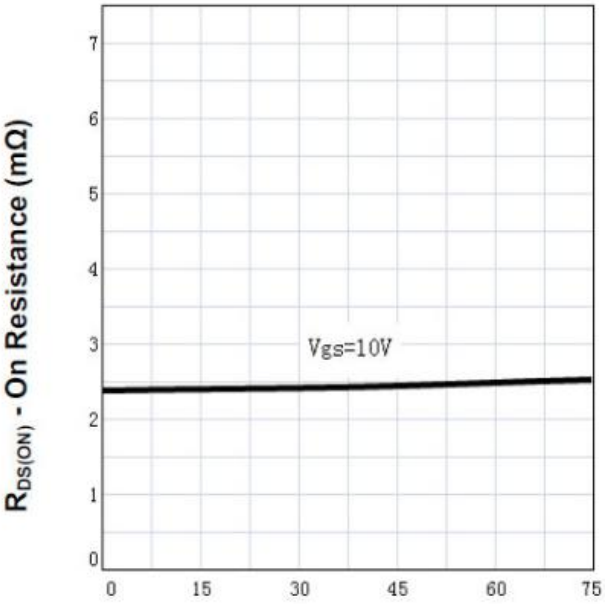




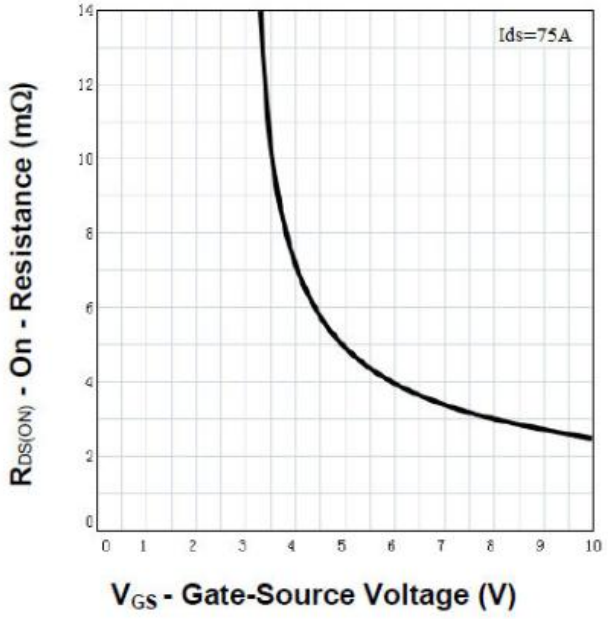
Output Characteristics



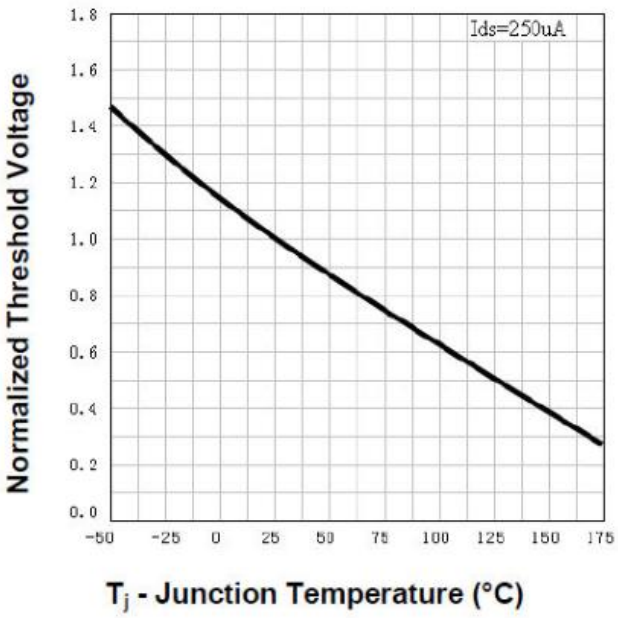
Drain-Source On Resistance



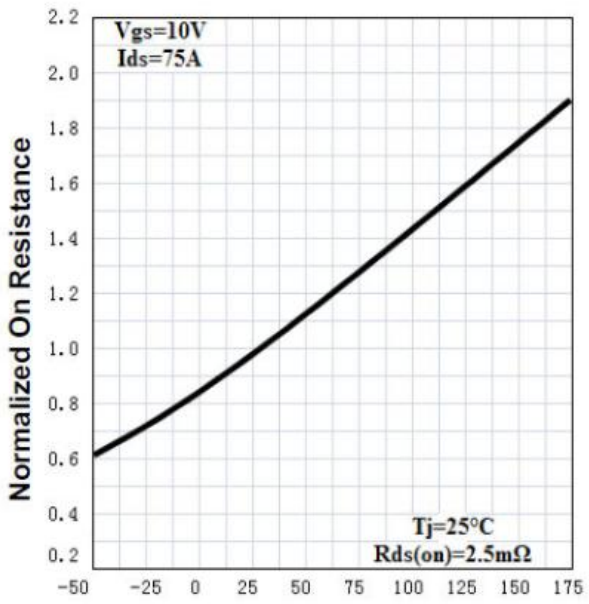
Drain-Source On Resistance



Gate Threshold Voltage

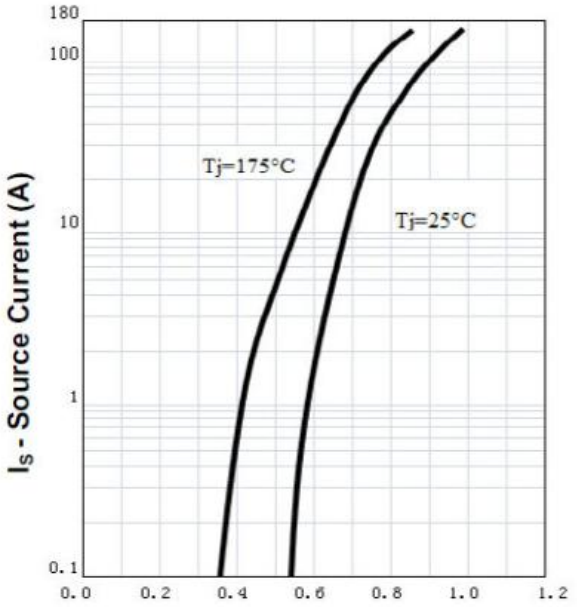


Drain-Source On Resistance



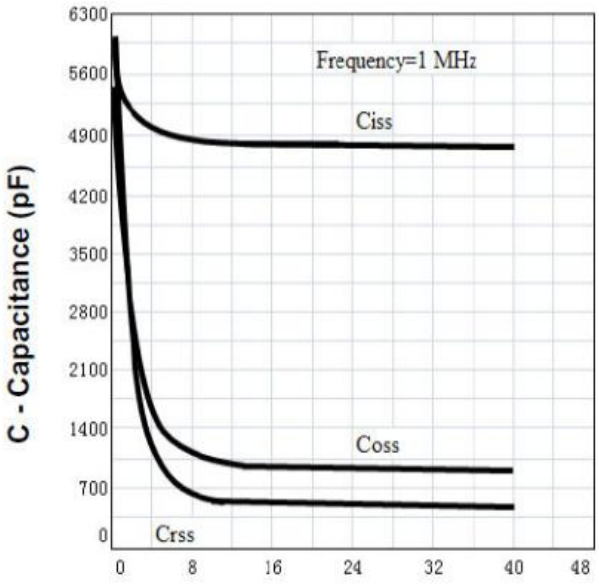
T_j - Junction Temperature (°C)

Source-Drain Diode Forward



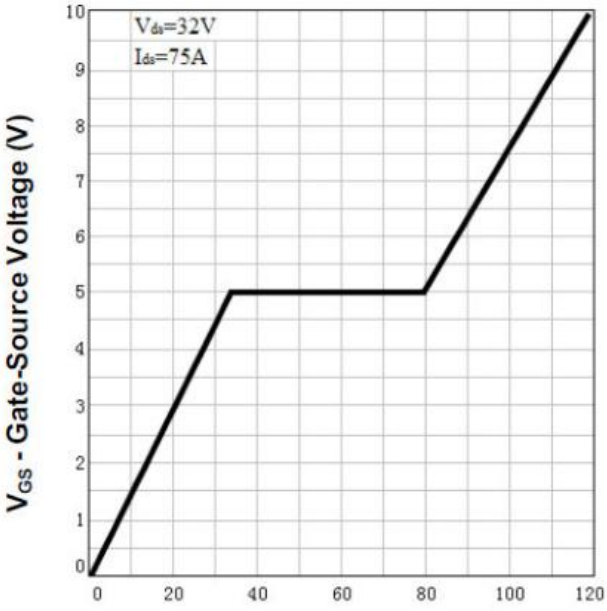
V_{SD} - Source-Drain Voltage (V)

Capacitance



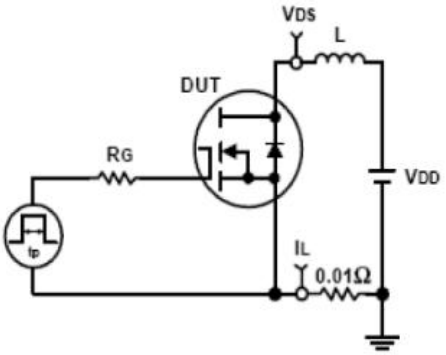
V_{DS} - Drain-Source Voltage (V)

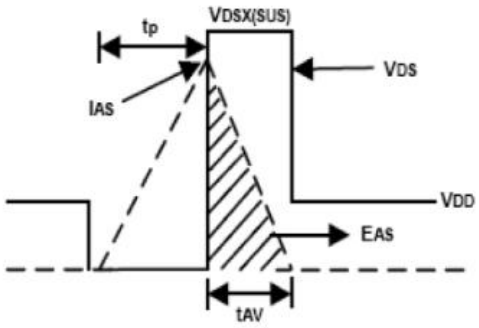
Gate Charge



Q_G - Gate Charge (nC)

Avalanche Test Circuit and Waveforms





Switching Time Test Circuit and Waveforms