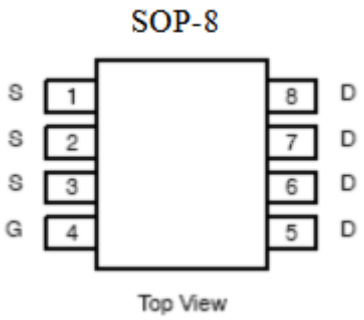
## 1. Features

- $R_{DS(on)}$=16mΩ(typ)@ $V_{GS}$=10 V
- Super low gate charge
- Green device available
- Excellent Cdv/dt effect decline
- Advanced high cell density trench technology

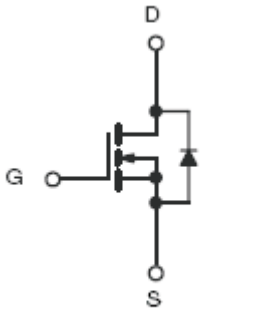
## 2.Description

The KIA4610A is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KIA4610A meet the RoHs and Green Product requirement.

## 3.Symbol



Top View



N-Channel MOSFET

## 4.Absolute maximum ratings

($T_A$=25°C,unless otherwise noted)

| Parameter | | Symbol | Rating | Units |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DSS}$ | 100 | V |
| Gate-source voltage | | $V_{GS}$ | ±20 | V |
| Continuous drain current $V_{GS}$@10V[1] | $T_A$=25ºC | $I_D$ | 7.5 | A |
| | $T_A$=70ºC | | 6 | |
| Pulsed drain current[2] | | $I_{DM}$ | 40 | A |
| Single pulse avalanche energy[3] | | EAS | 16 | mJ |
| Avalanche current | | $I_{AS}$ | 18 | A |
| Total power dissipation[4] | $T_A$=25ºC | $P_D$ | 2.5 | W |
| Junction and storage temperature range | | $T_J$ ,$T_{STG}$ | -55 to150 | ºC |
| Thermal resistance-junction to ambient[1] (t≤10s) | | $R_{\theta JA}$ | 50 | ºC/W |
| Thermal resistance-junction to ambient[1] (steady state) | | | 85 | ºC/W |

## 5.Electrical characteristics

($T_J$=25°C,unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Drain-Source breakdown voltage | $BV_{DSS}$ | $V_{GS}$=0V, $I_D$=-250μA | 100 | - | - | V |
| $BV_{DSS}$ Temperature coefficient | $\triangle BV_{DSS}/\triangle T_J$ | Reference to 25°C, $I_D$=1mA | - | 0.08 | - | V/°C, |
| Drain-Source Leakage Current | $I_{DSS}$ | $V_{DS}$=80V,$V_{GS}$=0V, $T_J$=25°C | - | - | 10 | μA |
| | | $V_{DS}$=80V,$V_{GS}$=0V, $T_J$=55°C | - | - | 100 | |
| Gate-source leakage current | $I_{GSS}$ | $V_{GS}$=±20V,$V_{DS}$=0V | - | - | ±100 | nA |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$, $I_D$=250μA | 1.2 | - | 2.5 | V |
| $V_{GS(th)}$ Temperature coefficient | $\triangle V_{GS(th)}$ | | - | 5.5 | - | mV/°C |
| Static drain-source on- resistance[2] | $R_{DS(on)}$ | $V_{GS}$=10V,$I_D$=7A | - | 16 | 20 | mΩ |
| | | $V_{GS}$=4.5V,$I_D$=5A | - | 19 | 25 | |
| Forward transcend ductance | $g_{FS}$ | $V_{DS}$=5V, $I_D$=7A | - | 24 | - | S |
| Diode forward voltage[2] | $V_{SD}$ | $V_{GS}$=0V,$I_S$=-1A, $T_J$=25°C | - | - | 1.2 | V |
| Gate resistance | $R_g$ | $V_{DS}$=0V, $V_{GS}$=0V,f=1MHz | - | 1.6 | - | Ω |
| Total gate charge(10V) | $Q_g$ | $V_{DS}$=80V, $V_{GS}$=10V $I_D$ =7A | - | 36 | - | nC |
| Gate-source charge | $Q_{gs}$ | | - | 5 | - | |
| Gate-drain charge | $Q_{gd}$ | | - | 10 | - | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$=50V, $R_G$=3.3Ω, $V_{GS}$=10V $I_D$=7A | - | 11.5 | - | ns |
| Rise time | $t_r$ | | - | 29 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 42 | - | |
| Fall time | $t_f$ | | - | 18 | - | |
| Input capacitance | $C_{iss}$ | $V_{GS}$=0V, $V_{DS}$=15V F=1.0MHZ | - | 1930 | - | pF |
| Output capacitance | $C_{oss}$ | | - | 245 | - | |
| Reverse transfer capacitance | $C_{rss}$ | | - | 125 | - | |
| Diode characteristics | | | | | | |
| Continuous source current[1.5] | $I_S$ | $V_G$=$V_D$=0V,Force current | - | - | 7 | A |
| Pulsed source current[2.5] | $I_{SM}$ | | - | - | 40 | A |
| Reverse recovery time | $t_{rr}$ | $I_F$=7A,dI/dt=100A/us, $T_J$=25°C | - | 48 | - | nS |
| Reverse recovery charge | $Q_{rr}$ | | - | 29 | - | nC |

Note:1. The data tested by surface mounted on a 1 inch$^2$ FR-4 board with 2OZ copper.

2. The data tested by pulsed, pulse width ≤300us,duty cycle ≤2%.

3. The EAS data shows Max.rating. The test condition is $V_{DD}$=25V, $V_{GS}$=10V, L=0.1mH,$I_{AS}$=18A.

4. The power dissipation is limited by 150 ºC junction temperature.

5. The data is theoretically the same as $I_D$ and $I_{DM}$, in real applications, should be limited by total power dissipation.

## 6. Test circuits and waveforms

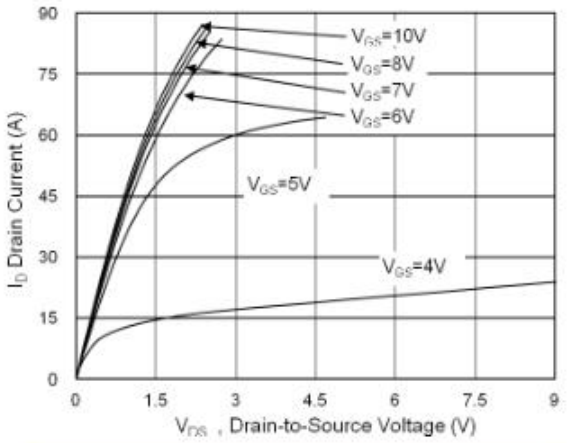



Fig.1 Typical Output Characteristics

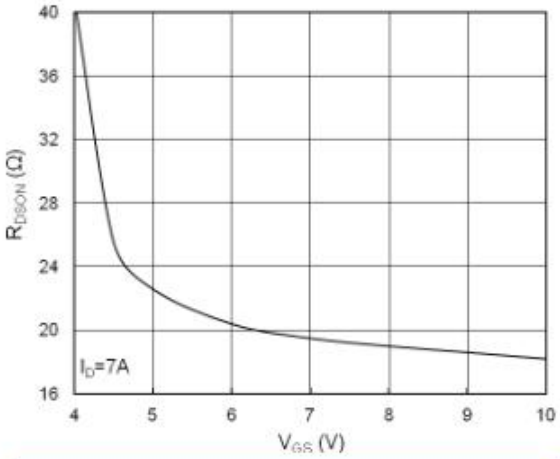



Fig.2 On-Resistance vs. Gate-Source

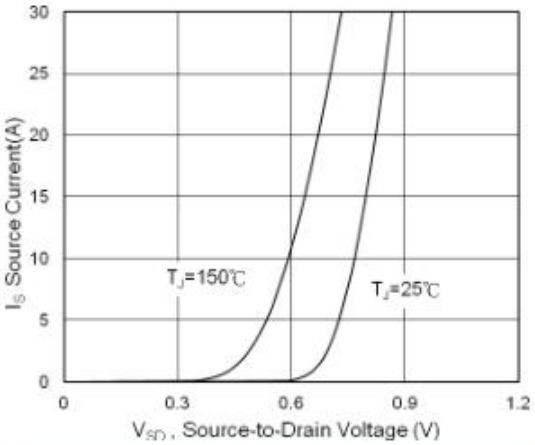



Fig.3 Forward Characteristics Of Reverse

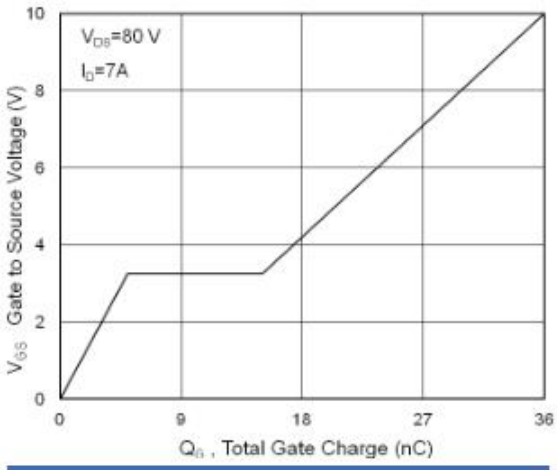



Fig.4 Gate-Charge Characteristics

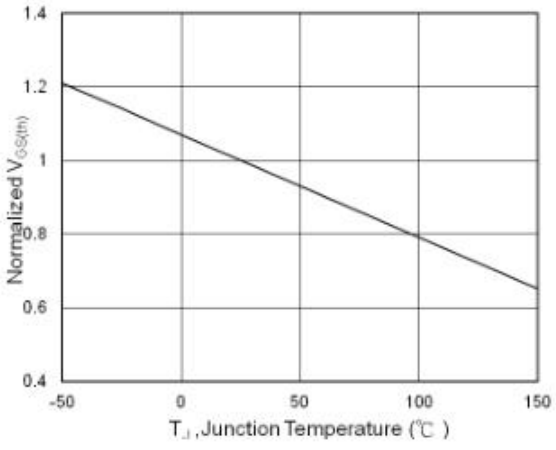



Fig.5 Normalized $V_{GS(th)}$ vs. $T_J$

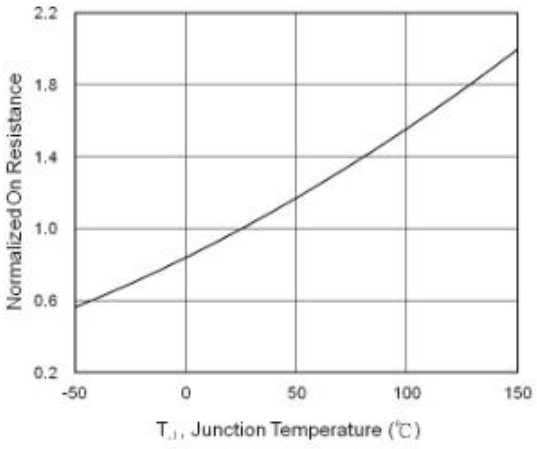



Fig.6 Normalized $R_{DSON}$ vs. $T_J$

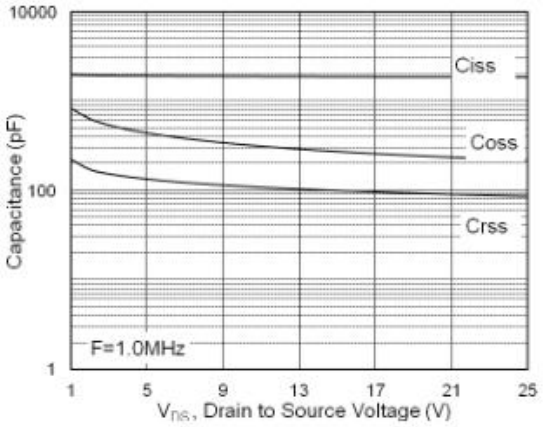



Fig.7 Capacitance

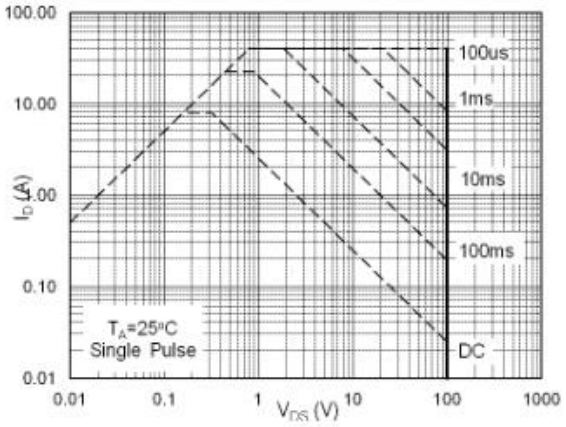



Fig.8 Safe Operating Area

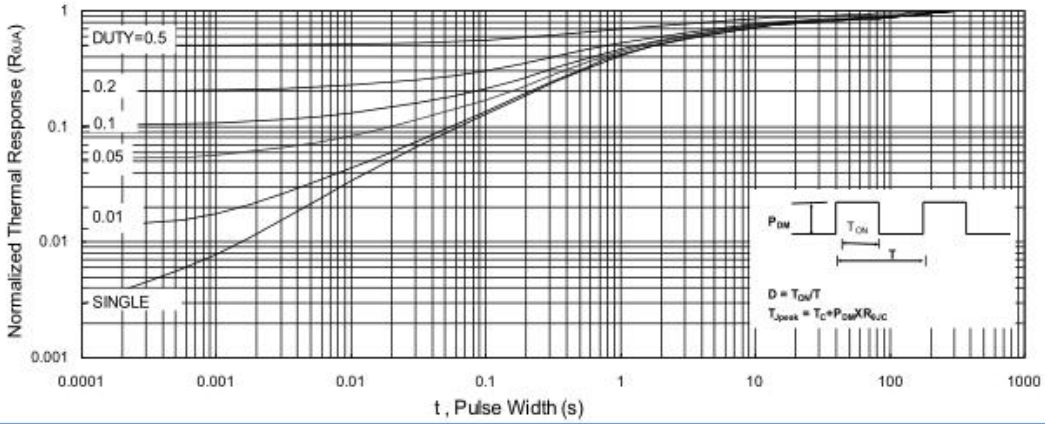



Fig.9 Normalized Maximum Transient Thermal Impedance

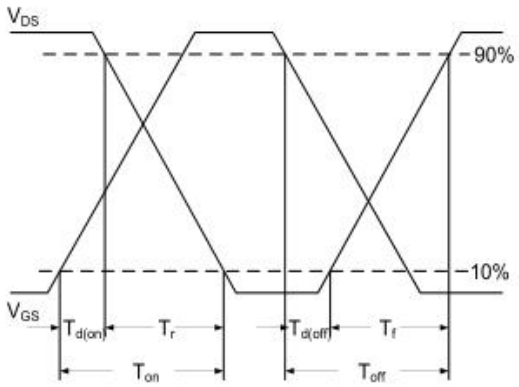



Fig.10 Switching Time Waveform

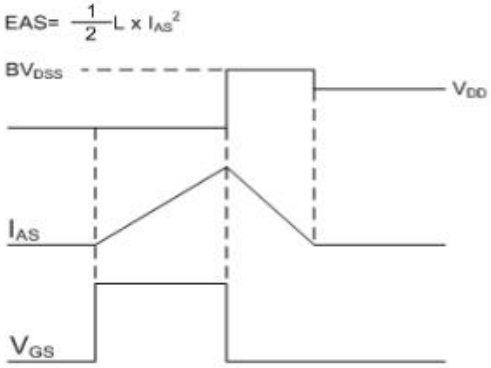



Fig.11 Unclamped Inductive Switching Waveform