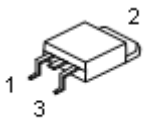
1. Features

- $R_{DS(on)}$=42mΩ(typ) @ V_{GS}=10V
- 100% EAS guaranteed
- *Pb−Free, RoHS Compliant*
- Super low gate charge
- Excellent Cdv/dt effect decline
- Advanced high cell density trench technology

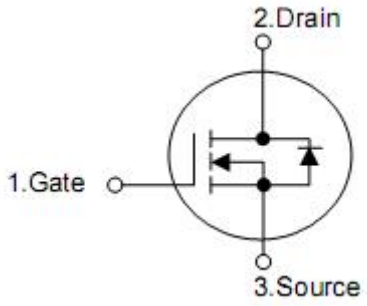
2.Description

The KPX8610C uses advanced trench MOSFET technology to provide excellent $R_{DS(ON)}$ and gate charge for use in a wide variety of other applications. The KPX8610C meet the RoHS and Green product requirememt, 100% EAS guaranteed with full function reliability approved.

3.Symbol



TO-252



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KPD8610C	TO-252	KIA

5.Absolute maximum ratings

Parameter		Symbol	Rating	Units
Drain-source voltage		V_{DS}	-100	V
Gate-source voltage		V_{GS}	±20	V
Continuous drain current V_{GS}@-10V[1]	T_C=25℃	I_D	-35	A
	T_C=100℃		-23	
Pulsed drain current[2]		I_{DM}	-100	A
Single pulse avalanche energy[3]		EAS	345	mJ
Avalanche current		I_{AS}	28	A
Total power dissipation[4]	T_A=25℃	P_D	104	W
Junction and storage temperature range		T_J ,T_{STG}	-55 to150	℃

6. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance,Junction-to-case[1]	R_{thJC}	1.2	℃/W
Thermal Resistance Junction-Ambient[1]	R_{thJA}	62	℃/W

7. Electrical characteristics

(T_J=25°C,unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-100	-	-	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-100V,V_{GS}=0V, T_J=25°C	-	-	-1	μA
Gate-source leakage current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	-1.0	-1.9	-3.0	V
Static drain-source on- resistance[2]	$R_{DS(on)}$	V_{GS}=-10V,I_D=-18A	-	42	55	mΩ
		V_{GS}=-4.5V,I_D=-12A	-	46	60	
Total gate charge	Q_g	V_{DS}=-10V, V_{GS}=-10V I_D =-15A	-	72	-	nC
Gate-source charge	Q_{gs}		-	18	-	
Gate-drain charge	Q_{gd}		-	50	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=-10V, R_G=3.3Ω, V_{GS}=-10V I_D=-18A	-	23	-	ns
Rise time	t_r		-	50	-	
Turn-off delay time	$t_{d(off)}$		-	26	-	
Fall time	t_f		-	38	-	
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-10V F=1.0MHZ	-	4060	-	pF
Output capacitance	C_{oss}		-	120	-	
Reverse transfer capacitance	C_{rss}		-	20	-	
Diode characteristics						
Continuous source current[1.5]	I_S	T_A=25℃	-	-	-35	A
Diode forward voltage[2]	V_{SD}	V_{GS}=0V,I_S=-20A, T_J=25°C	-	-	1.2	V

Note:1. Pulse width limited by maximum allowable junction temperature

2. The data tested by pulsed, pulse width ≤300us,duty cycle ≤2%.

3. The EAS data shows Max.rating. The test condition is V_{DD}=-50V, V_{GS}=-10V, L=0.88mH.I_{AS}=-28A.

4. The power dissipation is limited by 150 °C junction temperature.

5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

8. Test circuits and waveforms

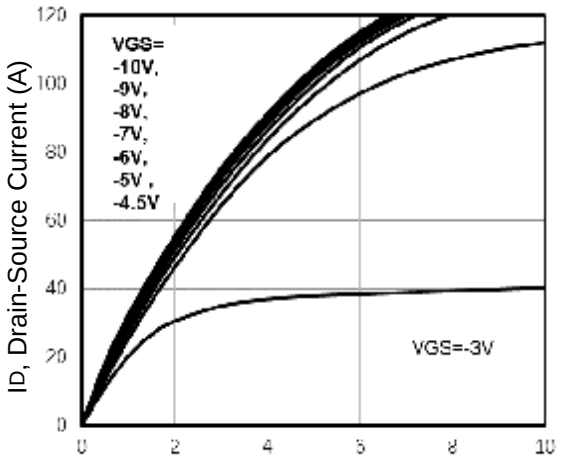


Fig1. Typical Output Characteristics

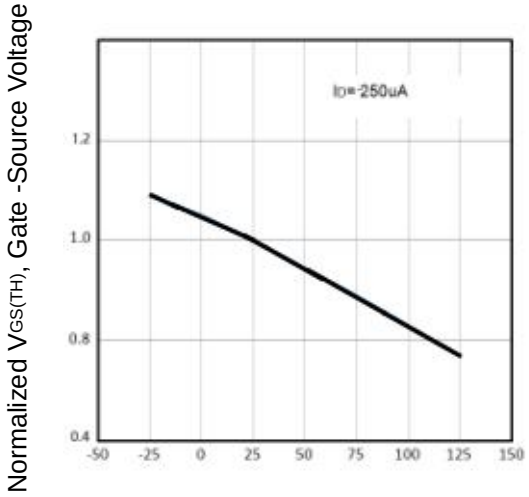


Fig2. Normalized Threshold Voltage Vs. Temperature

Tc, Case Temperature (° C)

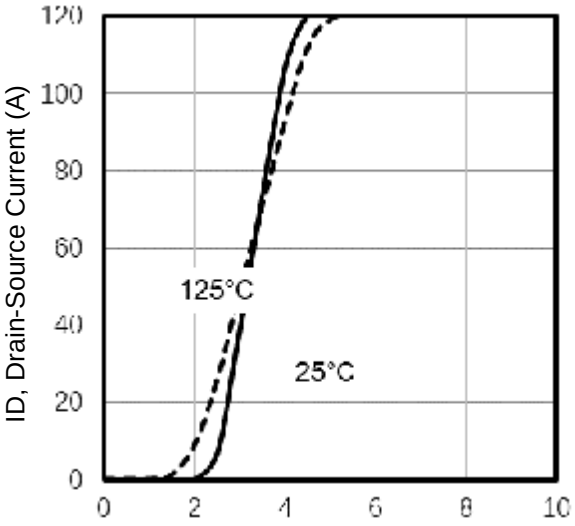


Fig3. Typical Transfer Characteristics

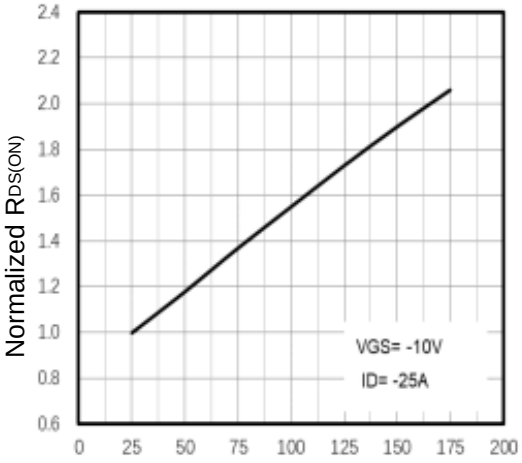


Fig4. Normalized Threshold Voltage Vs. Temperature

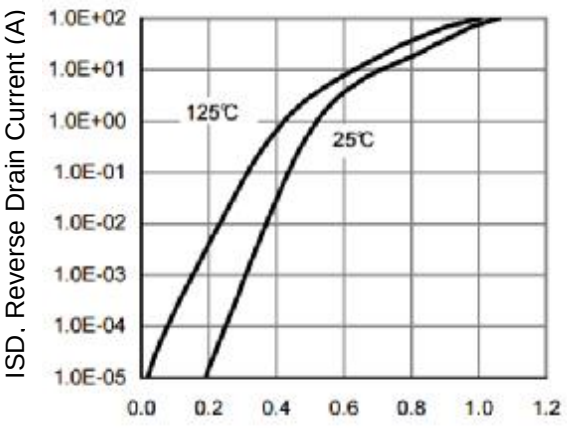


Fig5. Typical Source-Drain Diode Forward Voltage

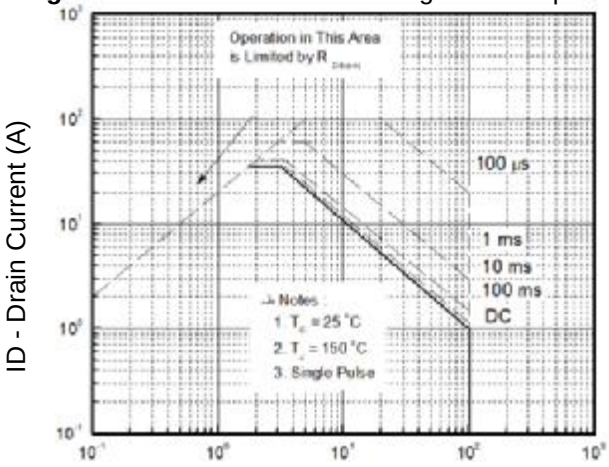


Fig6. Maximum Safe Operating Area

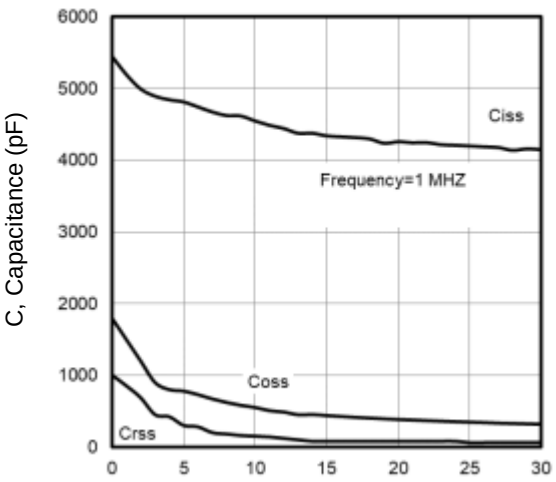


Fig7. Typical Capacitance Vs. Drain-Source Voltage

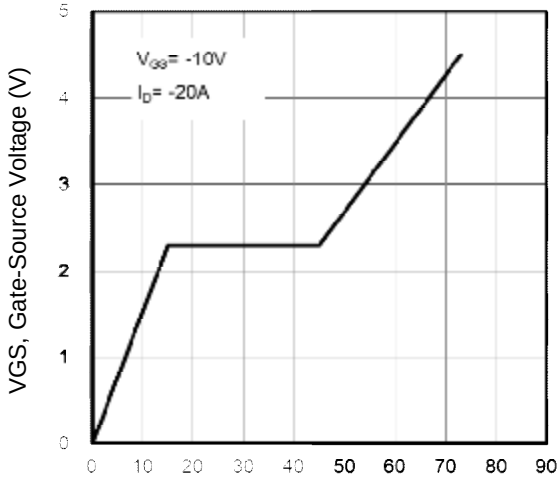


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

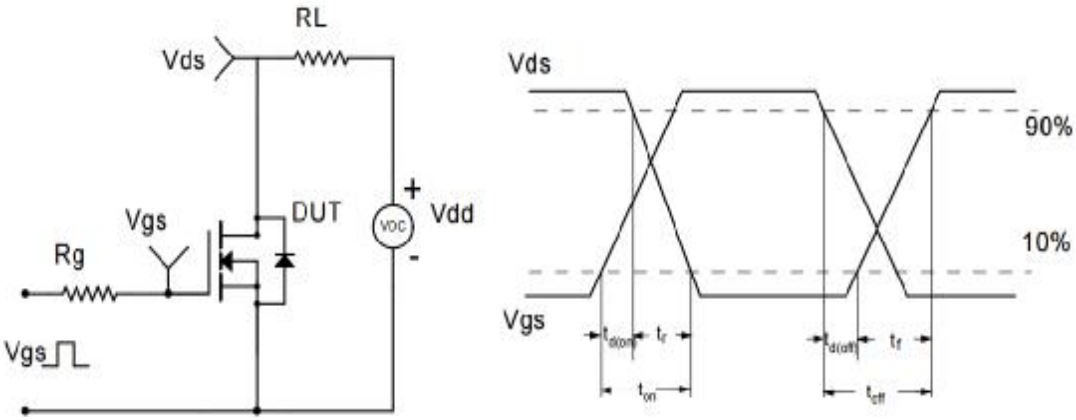


Fig10. Switching Time Test Circuit and waveforms